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EXAMINER	
HUISMAN, DAVID J	

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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

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Office Action Summary	Application No. 09/598,713	Applicant(s) DOUGLAS, JONATHAN P.
	Examiner David J. Huisman	Art Unit 2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-7,9-12 and 17-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-7,9-12 and 17-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1, 4-7, 9-12, and 17-26 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: #7. Amendment "B" as received on 12/19/2003.

Claim Objections

3. Claim 10 recites the limitation "the return instruction" in the second to last line. There is insufficient antecedent basis for this limitation in the claim. Please replace "a new instruction" with --a return instruction-- in line 4.

4. Claim 11, is objected to because of the following minor informalities: Insert a colon after "comprising" in line 1. Furthermore, claim 11 recites the limitation "the external resource." There is insufficient antecedent basis for this limitation in the claim. Please replace "the external resource" with --the return stack buffer--. Finally, if applicant agrees with the objection of claim 10, then claim 11 is also objected to. More specifically, the applicant should replace both instances of "the new instruction" with --the return instruction--.

5. Claim 18 is objected to because of the following informalities: The examiner recommends that the applicant insert --at least-- before "one pipestage" in lines 3 and 6 of claim 18 to make it consistent with claim 17. Appropriate correction is required.

6. Claim 19 is objected to because of the following informalities: The examiner recommends that the applicant insert --at least-- before "one pipestage" in lines 3 and 6 of claim 19 to make it consistent with claim 17. Appropriate correction is required.

7. Claim 22 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. More specifically, the applicant has accidentally left claim 22 unfinished.

Maintained Rejections

8. Since no arguments have been presented, the applicant has failed to overcome the rejections set forth in the previous Office Action, for claims 17-20, which are respectfully maintained by the examiner and copied below for applicant's convenience.

Maintained Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pickett, U.S. Patent No. 5,968,169, as applied above, in view of Sproch et al., U.S. Patent No. 6,247,134 (herein referred to as Sproch).

11. Referring to claim 17, Pickett has taught execution logic for a processor comprising:

a) a first instruction pipe, comprising a first plurality of cascaded pipestages. See Fig.15 and note the cascaded stages of the pipeline (a new stage per clock cycle). The first pipe would include one of the multiple decode units and multiple functional units in order to operate on one many instructions fetched per clock cycle. See column 18, lines 31-38. Note that up to 6 instructions can be passed to 6 pipelines (Fig.1, components 208, 210, 212).

b) a return stack buffer (RSB) provided in communication with at least one of the first pipestages. See Fig. 2 and note that the decode units from each pipeline will communicate with the RSB.

c) a second instruction pipe, comprising:

c1) a second plurality of cascaded pipestages, at least one of the second plurality of pipestages provided in communication with the return stack buffer. Note that a second pipeline would include a second set among the decode units, functional units, etc. This pipeline would also have pipestages as shown in Fig.15. Also, recall from Fig.2, that each pipeline's decode unit will communicate with the RSB.

c2) Pickett has not explicitly taught clock throttling logic couple to the at least one second pipestage. However, Sproch has taught such a concept. See Fig.5. This circuitry takes in a clock signal and modifies the output clock signals based on the need for a stall. Also, see column 8, lines 50-61. The abstract of Sproch shows that such a concept allows for power saving within the pipeline. Therefore, in order to save power, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify

Pickett to include clock throttling logic as taught by Sproch. It should also be noted from Fig.5 that this logic is coupled to at least one pipestage of a pipeline.

12. Referring to claim 18, Pickett in view of Sproch has taught logic as described in claim 17. Sproch has further taught that the clock throttling logic comprises:

a) a state machine coupled to an output of the one pipestage from the second plurality of pipestages. See Fig.5 and note that state machine 210 is coupled to the first stage of a pipeline. It determines whether to stall a pipeline or not (2-state state machine).

b) a clock control circuit having an input for a system clock signal and having an output for a modified clock signal, the output coupled to the one pipestage, the clock control circuit controlled by the state machine. See Fig.5 and see components 351, 352, 353, 355, 362, 363, and 365. These components represent the innards of component 230, shown in Fig.3. This circuitry takes in a clock signal and modifies the output clock signals based on the state machine circuit 210. Also, see column 8, lines 50-61.

13. Referring to claim 19, Pickett in view of Sproch has taught logic as described in claim 17. Furthermore, claim 19 is the same as claim 18 except that the state machine is coupled to at least one of the first plurality of pipestages in claim 19 as opposed to the at least one of the second plurality of pipestages in claim 18. However, one of ordinary skill in the art would have recognized that if each pipeline were to include the ideas taught by Sproch, then each pipeline would be able to save power, resulting in more overall system power being saved. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Pickett to have a state machine coupled to the first plurality.

14. Referring to claim 20, Pickett in view of Sproch has taught logic as described in claim 17. Pickett has further taught that additional instruction pipestages from either the first or the second instruction pipe are provided in communication with the return stack buffer, the additional instruction pipestages also provided with additional clock throttling logic. Recall from above that the decode units (which operate in decode stages of pipelines) communicate with the RSB via selector 258 as shown in Fig.2. In addition, as shown in Fig.2 and Fig.4, when a return address is selected from the stack it is applied to the instruction cache as a fetch address. Therefore, the RSB is also in communication with the fetch stage of the pipelines since a return address is a fetch address. In addition, it should be noted from Sproch that the clock throttling logic, which is used to save power, is coupled to each of the pipeline stages.

New Claim Rejections - 35 USC § 102

15. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

16. Claims 1, 6, 10-12, and 21-22 are rejected under 35 U.S.C. 102(b) as being anticipated by IBM Technical Disclosure Bulletin NN9204269 (herein referred to as IBM). Furthermore, Hennessy and Patterson, Computer Architecture - A Quantitative Approach, 2nd Edition, 1996 (as applied in the previous Office Action and herein referred to as Hennessy), has been provided as extrinsic evidence showing that a stall inherently stalls pipeline stages before the stalled pipestage.

17. Referring to claim 1, IBM has taught an instruction pipe control method comprising:

a) reading a return instruction from an instruction pipestage. Throughout IBM, pipeline stages, such as a decode stage and write-back stage are disclosed, showing that IBM's system is indeed pipelined. And, in a pipelined system, instructions are inherently read from instruction pipestages.

b) determining, with reference to other instructions read previously from the instruction pipestage, whether a return address associated with the return instruction can be written immediately to a next instruction pipestage and stalling processing of the return instruction until the return address associated with the return instruction is read from an external resource. See page 3 regarding the situation where a return instruction closely follows a call instruction. IBM has disclosed that in this situation, the return instruction must be stalled until the call instruction completes (during the write-back stage when the address is pushed onto the stack). If the return were not stalled, then one of ordinary skill in the art would realize that an incorrect return address would be prefetched from the stack (as discussed on page 2).

18. Referring to claim 6, IBM has taught a method as described in claim 1. Furthermore, it is the inherent nature of a stall to stall the instruction pipestage and all other instruction pipestages before it in the instruction pipe. For instance, see Figure 3.13 on page 154 and note that if the SUB instruction is stalled before its 3rd stage (as shown), then the next two subsequent instructions are stalled before their 2nd and 1st stages respectively.

19. Referring to claim 10, IBM has taught a method for interfacing an instruction pipe with a return stack buffer having a predetermined round-trip communication latency period associated with a communication path therebetweeen, the method comprising:

a) reading a new instruction from an instruction pipe stage. Throughout IBM, pipeline stages, such as a decode stage and write-back stage are disclosed, showing that IBM's system is indeed pipelined. And, in a pipelined system, instructions are inherently read from instruction pipestages.

b) determining, with reference to other instructions read previously from the instruction pipestage, whether a return address is available to the instruction pipe prior to expiration of the round-trip communication latency period with the return stack buffer, and if not, stalling processing of the return instruction until the round-trip communication latency period expires. See page 3 regarding the situation where a return instruction closely follows a call instruction. IBM has disclosed that in this situation, the return instruction must be stalled until the call instruction completes the pushing of the return address onto the stack (which occurs during the writeback stage). If the return were not stalled, then one of ordinary skill in the art would realize that an incorrect return address would be prefetched from the stack (as discussed on page 2). It should be realized that in order for the instruction to push an address onto the stack, there must inherently be a communication path between the pipe and the stack. And, the amount of time it takes for the push to occur is the predetermined round-trip communication latency. Therefore, the return must be stalled until the communication latency (push) expires.

20. Referring to claim 11, IBM has taught a method as described in claim 10. IBM has further taught determining whether the return instruction requires access to the return stack buffer in excess of an access allocation for the instruction piper, and if so, stalling the return instruction. Looking at page 3 of IBM, it is explained that if two return instructions are close to each other, then the second will have to be stalled since only one should access the stack at a

time. More specifically, the first return must be able to pop the stack before the second return reads from the stack. Otherwise, the second return will retrieve the wrong address.

21. Referring to claim 12, IBM has taught a method as described in claim 10. Furthermore, it is the inherent nature of a stall to stall the instruction pipestage and all other instruction pipestages before it in the instruction pipe. For instance, see Figure 3.13 on page 154 and note that if the SUB instruction is stalled before its 3rd stage (as shown), then the next two subsequent instructions are stalled before their 2nd and 1st stages respectively.

22. Referring to claim 21, IBM has taught a method as described in claim 1. IBM has further taught that when the return address is immediately available, reading the return address from storage in the pipestage to the next pipestage. See pages 1 and 2 and the figure of IBM. From the explanation, it should be realized that IBM has disclosed a stack cache (comprising registers RTN 1-3), which holds the 3 most recent return addresses within the system. This allows for fetching of instructions starting at the most recent return address to occur sooner (prefetching) since the system will not have to wait for the stack to be popped in order to retrieve the address.

23. Referring to claim 22, IBM has taught a method as described in claim 1. Furthermore, since claim 22 fails to further limit claim 1, claim 22 is rejected for the same reasons set forth in the rejection of claim 1.

24. Claim 23 is rejected under 35 U.S.C. 102(b) as being anticipated by Hoyt et al., U.S. Patent No. 5,604,877 (as applied in the previous Office Action and herein referred to as Hoyt).

25. Referring to claim 23, Hoyt has taught an instruction control method, comprising, responsive to a return instruction in a first pipestage of an instruction pipe:

a) determining whether a return address associated with the return instruction is stored in a register locally within the pipestage, and if so, passing the return address from the register to a next pipestage. See column 10, lines 55-58, and note that when a return instruction is encountered, it is determined whether or not an appropriate address is stored in the return register (Fig.5, component 45). If a valid address does exist within that register, then it will be passed on and used as a prediction.

b) if not, retrieving the return address from a return stack buffer and stalling operation of all pipestages downstream of the first pipestage until the return address is received from the return stack buffer. See column 10, lines 62-65, and note that if a valid address is not stored in the return register, then the stack is accessed (Fig.5, component 51). Furthermore, from column 2, lines 20-36, it is disclosed that it is desirable to predict return addresses so that the stack in memory does not have to be accessed. However, when this prediction is not valid, the stack must be accessed and a stall will occur for as long as that access takes. In addition, it is the inherent nature of a stall to stall all pipeline stages downstream from the first pipestage.

New Claim Rejections - 35 USC § 103

26. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

27. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pickett, as applied above, in view of Hennessy, as applied above.

28. Referring to claim 4, Pickett has taught an instruction pipe control method comprising:

a) reading a call instruction from an instruction pipestage. Note from Fig.15, for instance, that the system is pipelined. And, in a pipelined machine, instructions are read from instruction pipestages. In addition, from the abstract, Pickett has disclosed that call instructions exist within the system.

b) Pickett has not explicitly taught determining, with reference to other instructions read previously from the instruction pipestage, whether immediate processing of the call instruction would exceed a predetermined access rate of the instruction pipe to a return stack buffer, and stalling processing of the call instruction until sufficient time has expired to synchronize processing of the call instruction with the predetermined access rate. However, Hennessy has taught the general idea of structural hazards on page 141, which is a hazard caused by a combination of instructions that cannot be accommodated because of resource conflicts. Hennessy further gives an example of a pipeline trying to perform two register-file writes to a register-file with a single write port. Since both writes cannot be accommodated, a structural hazard exists and one of the instructions must be stalled until the other write finishes. This situation is directly applicable to Pickett in that multiple pipelines are share a return stack. See Fig.1 and Fig.2. However, as is known in the art (and supported by Pickett in column 1, lines 62-67), a call instruction results in an address being pushed (written) on the stack. If two call instructions are executed at the same time, then two pushes to the stack (two writes) will need to be performed at the same time. However, this is not possible because with a stack, the only place to write is at the top of the stack. And, if both calls are allowed to write to the top of the stack, one of the values will be overwritten. Therefore, if immediate processing of a call

instruction would exceed a predetermined access rate to a return stack buffer (in this case, one write at a time), then the call instruction must be stalled until sufficient time has expired. This will ensure that both calls are executed correctly. As a result, in order to ensure correct execution, it would have been obvious to one of ordinary skill in the art at the time of the invention to stall a call instruction if the immediate processing of that call instruction would exceed a predetermined access rate to a return stack buffer.

29. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pickett in view of Hennessy, as applied above, and further in view of Hoyt, as applied above.

30. Referring to claim 5, Pickett in view of Hennessy has taught an instruction pipe control method as described in claim 4. Pickett in view Hennessy has not explicitly taught after the stalling terminates, storing a return address associated with the call instruction both locally and in a shared resource. However, Hoyt has taught a system for predicting return addresses wherein the prediction is made using either a register within the pipeline (Fig.5, component 45), or using a return stack buffer (Fig.5, component 51), which is normally implemented as a LIFO in main memory (column 2, lines 20-36). Hoyt has disclosed (in the Background section) that performing such prediction improves the efficiency of the system in that the processor can continue fetching instructions down the predicted path, thereby keeping the pipeline full. This advantage is also recognized by Hennessy (as shown in Figure 3.26 on page 167). Therefore, in order to aid in the prediction of return addresses, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Hennessy such that it is capable of predicting such addresses, as taught by Hoyt. And, part of this prediction system includes

storing a return address both locally (in register 45, Fig.5) and in a shared resource (stack 51, Fig.5), where the return stack buffer is shared by components 40 and 60 (decoder and branch target buffer circuit). By storing the prediction locally, the prediction could be accessed more quickly as opposed to retrieving the prediction from the return stack buffer in memory. However, the return addresses must also be stored in the stack since the register can only hold one prediction. If there were no stack, then the system would lose return predictions if two or more calls happen in a row before a return. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to store the address both locally and in a shared resource.

31. Claims 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hennessy, as applied above, in view of Hoyt, as applied above.

32. Referring to claim 7, Hennessy has taught an interface method for an instruction pipe that shares access to an external resource, comprising:

a) reading a call instruction from an instruction pipestage. Note that Hennessy has taught a call instruction on page 277. Furthermore, it should be realized that all instructions are read from an instruction pipestage. For instance, every instruction which is to be executed will inherently have to be fetched first (fetch stage).

b) determining with reference to other instructions read previously from the instruction pipestage, whether immediate processing of the call instruction would cause the instruction pipe to exceed the instruction pipe's access allocation to the external resource. See page 142, Figure 3.6. In this particular figure, if Instruction 3 were a call instruction, the immediate processing of

the call would cause a structural hazard with the load instruction since both are accessing a memory, which is shared by the fetch and memory stages of the pipeline. In this case, the immediate processing of the call would exceed a predetermined access rate associated with the memory. That is, the pipe is only allowed to make one request to memory at a time and in the above example, two requests would be made (one from the "Load" instruction to load data from memory and the second from Instruction 3 to fetch the call instruction).

c) if so, stalling the new instruction. See page 143, Figure 3.7. Note that the structural hazard is dealt with by stalling.

d) Hennessy has not taught that after the stalling terminates, storing a return address associated with the call instruction both locally and in a shared resource. However, Hoyt has taught a system for predicting return addresses wherein the prediction is made using either a register within the pipeline (Fig.5, component 45), or using a return stack buffer (Fig.5, component 51), which is normally implemented as a LIFO in main memory (column 2, lines 20-36). Hoyt has disclosed (in the Background section) that performing such prediction improves the efficiency of the system in that the processor can continue fetching instructions down the predicted path, thereby keeping the pipeline full. This advantage is also recognized by Hennessy (as shown in Figure 3.26 on page 167). Therefore, in order to aid in the prediction of return addresses, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Hennessy such that it is capable of predicting such addresses, as taught by Hoyt. And, part of this prediction system includes storing a return address both locally (in register 45, Fig.5) and in a shared resource (stack 51, Fig.5), where the return stack buffer is shared by components 40 and 60 (decoder and branch target buffer circuit). By storing the prediction locally, the prediction

could be accessed more quickly as opposed to retrieving the prediction from the return stack buffer in memory. However, the return addresses must also be stored in the stack since the register can only hold one prediction. If there were no stack, then the system would lose return predictions if two or more calls happen in a row before a return. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to store the address both locally and in a shared resource.

33. Referring to claim 9, Hennessy in view of Hoyt has taught a method as described in claim 7. Hennessy has further taught that the stalling stalls the instruction pipestage and all other instruction pipestages before it in the instruction pipe. See Figure 3.13 on page 154 and note that if the SUB instruction is stalled before its 3rd stage (as shown), then the next two subsequent instructions are stalled before their 2nd and 1st stages respectively.

34. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hoyt, as applied above, in view of IBM, as applied above.

35. Referring to claim 24, Hoyt has taught a method as described in claim 23. Hoyt has not explicitly taught the specifics of claim 24. However, IBM has taught that if the pipestage processed a prior return instruction within a number of clock cycles that are fewer than a number of clock cycles that are required for round trip communication between the pipestage and the return stack buffer, then stalling the downstream pipestages until the number of clock cycles since processing of the prior return instruction equals the number of clock cycles required for round trip communication. See page 3 of IBM and note that when a second return closely follows a first return, the second return must be stalled until the first return completes by popping

its corresponding return address off of the return stack. The round trip communication would be the time it takes for the first return to pop the stack and clearly, the second return will have to wait until that communication is complete. Furthermore, it is the inherent nature of a stall to stall all pipeline stages downstream from the first pipestage.

36. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hoyt, as applied above, in view of Cosgrove et al., U.S. Patent No. 4,399,507 (herein referred to as Cosgrove).

37. Referring to claim 25, it should be realized that the basic functionality of claim 25 has been anticipated by Hoyt. In fact, the only difference between applicant's claim 25 and Hoyt is that Hoyt does not employ a second register. Instead, the return stack buffer is coupled to the selector without the use of an intermediate register. More specifically, Hoyt has taught an instruction pipe comprising:

a) a plurality of pipestages connected in cascade. See Fig.1.

b) Hoyt has taught a first register to store a return address received from the first pipestage during receipt of a call instruction. See Fig.5, component 45, and column 10, lines 4-10. However, Hoyt has not explicitly taught a second register to store a return address received from a return stack buffer. However, Cosgrove has taught such a register. See Fig.3, component 18, and column5, lines 29-46. Note that when a return instruction is encountered, a return address is retrieved from the stack and stored in register 18. This allows quick address access for a next return instruction to quickly. As a result, in order to make an address available immediately, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Hoyt to include a second register as taught by Cosgrove.

c) Hoyt has taught a selector for choosing between multiple return addresses. See Fig.5 and note the selector that has inputs coupled to register 45 and return stack buffer 51. Since it has been determined that it would have been obvious to one of ordinary skill in the art at the time of the invention to implement a second register to hold values from the return stack buffer, then it would be further obvious to have the selector coupled to the second register.

38. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hoyt in view of Cosgrove, as applied above, and further in view of Sproch et al., as applied above.

39. Referring to claim 26, Hoyt in view of Cosgrove has taught an instruction pipe as described in claim 25. Furthermore, although Hoyt in view of Cosgrove must inherently include pipeline stall circuitry, they have not explicitly taught a clock stopping circuit to control the second pipestage and pipestages downstream therefrom. However, Sproch has taught such circuitry. See Fig.5, and note the circuitry comprising components the AND gates, the flip-flops, the clock, and the stall circuit 210. This circuitry controls whether the clock is applied to each of the pipeline stages 221-225. Also, see column 8, lines 50-61 and note that the pipestages downstream are also controlled. The abstract of Sproch shows that such a concept allows for power saving within the pipeline. Therefore, in order to save power, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Hoyt in view of Cosgrove to include clock stopping logic as taught by Sproch.

Response to Arguments

40. Applicant's arguments with respect to claims 1, 3, 4-6, and 10-12 have been considered but are moot in view of the new ground(s) of rejection.

41. In the remarks, Applicant argues the novelty/rejection of claim 7 on page 9 of the remarks, in substance that:

> "Neither reference teaches or suggests storing a return address in two places, a local place and a shared resource."
>
> "Applicant's respectfully suggest that the office action's analysis with respect to prediction of return addresses does not apply to processing of call instructions. Prediction occurs to speed processing of a return instruction."

42. These arguments are not found persuasive for the following reasons:

a) Regarding the first argument, Hoyt has taught storing a return address in a local place and a shared resource. See Fig.5 of Hoyt and the abstract. Note that the return addresses are stored in both the return register 45 and the RSB 51.

b) Regarding the second argument, the examiner agrees that prediction is involved with return instructions. However, this is the reason that the examiner has combined Hennessy and Hoyt. Hoyt has taught storing a return address locally and in a shared resource. And, this is an obvious improvement in Hennessy because it would allow Hennessy's system to predict return addresses. Hoyt's system is related to a call instruction because the call is what causes a return address to be written both locally and in a shared resource. In essence, it would be obvious to modify Hennessy in view of Hoyt so that when a call instruction is encountered, a return address is written both locally and in a shared resource. This in turn allows for fast prediction when a return instruction is encountered.

Conclusion

43. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

Yamamoto et al., U.S. Patent No. 6,170,998, has taught a processor which returns from a subroutine at high speed and a program translating apparatus which generates machine programs that make a high speed return from a subroutine. Yamamoto also discloses a pipeline register used to hold return addresses to try and prevent long delays due to stack access.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (703) 305-7811. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

DJH
David J. Huisman
January 21, 2004

Eddie Chan

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